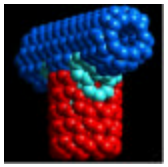
Nanotechnology in Information Processing: Opportunities and Challenges



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3rd NASA/DoD Workshop on Evolvable Hardware, Long Beach, CA
July 12, 2001, Keynote Talk

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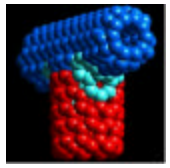
Acknowledgement



- M. Anantram
- Deepak Srivastava
- Toshi Yamada
- Jie Han
- Chongwu Zhou (USC)

Special thanks are due to Prof. Charles Lieber (Harvard) for sharing his novel and revolutionary concepts on Nanoelectronics and providing viewgraphs.

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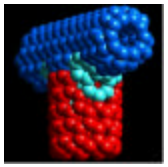
Outline



- Introduction
- Carbon nanotubes in nanoelectronics
- Nanowires
- Organic molecules
- Systems and Architechures
- Summary

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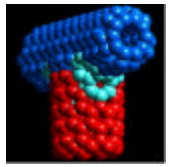
What is Expected from Alternative Technologies?



- Must be easier and cheaper to manufacture than CMOS
- Need high current drive; should be able to drive capacitances of interconnects of any length
- High level of integration (10^9 transistors/circuit)
- High reproducibility (better than ± 5%)
- Reliability (operating time > 10 years)
- Very low cost (< 1 µcent/transistor)
- Everything about the new technology must be compelling and simultaneously further CMOS scaling must become difficult and not cost-effective. If these two do not happen together, the enormous infrastructure built around silicon will make it difficult for alternatives to emerge.

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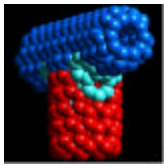
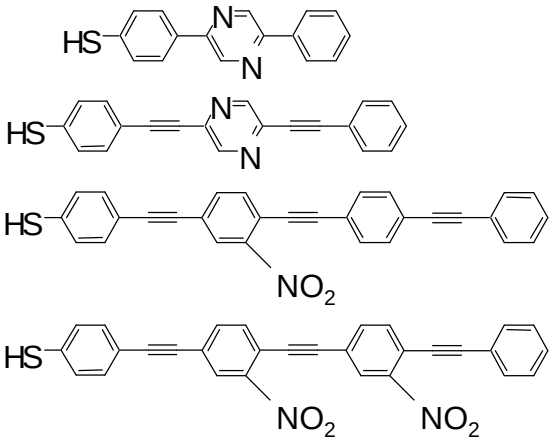
Molecular Electronics



Four possible avenues

- Semiconducting single wall carbon nanotubes
- Organic Molecular wires
- Nanowires (Si, GaAs, InP...)
- Biomolecules (DNA)



Examples of the SAM molecular materials to be used in the proposed work. SH is the substrate binding group, which will be chosen to form a strong bond to the Au substrate.

NASA Ames design

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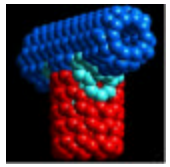
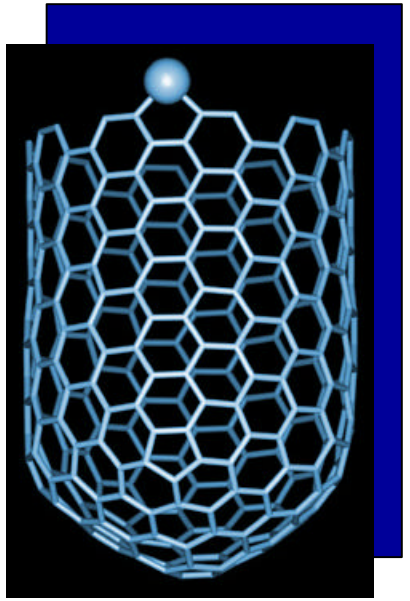
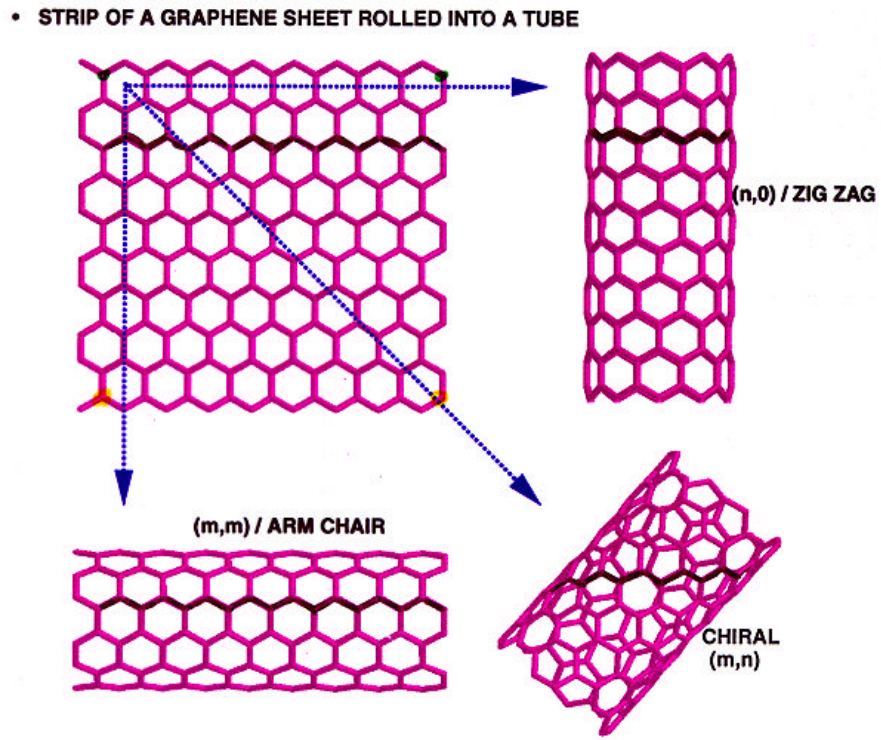
Carbon Nanotube



CNT is a tubular form of carbon with diameter as small as 1 nm.
Length: few nm to microns.

CNT is configurationally equivalent to a two dimensional graphene sheet rolled into a tube.





CNT exhibits extraordinary mechanical properties: Young's modulus over 1 Tera Pascal, as stiff as diamond, and tensile strength ~ 200 GPa.

CNT can be metallic or semiconducting, depending on chirality.

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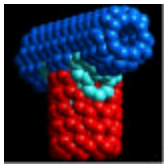
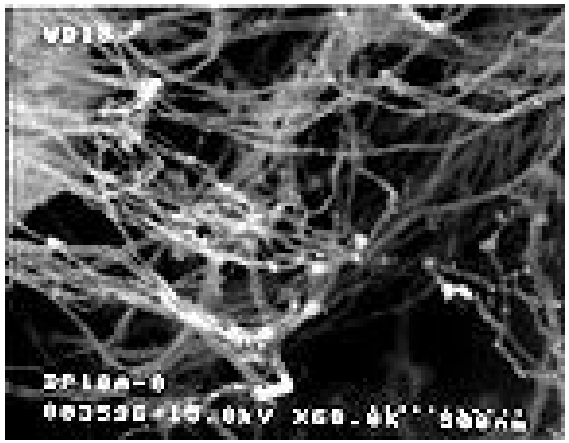
Attractive Properties of CNT



- Can be metallic or semiconducting depending on chirality. Recent work shows that functionalization with F atom leads to dielectric character. Entire transistor based on one material?
- Electronic properties can be tailored through application of external magnetic field, introduction of mechanical deformation…
- Exceptional mechanical strength
- High aspect ratio and small tip radius of curvature are ideal for field emission
- Site-dependent (or kinky) chemistry - enhanced chemical reactivity in regions of local conformation strain - is suitable for functionalization needed for many applications
- High thermal conductivity in the axial direction



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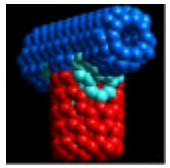
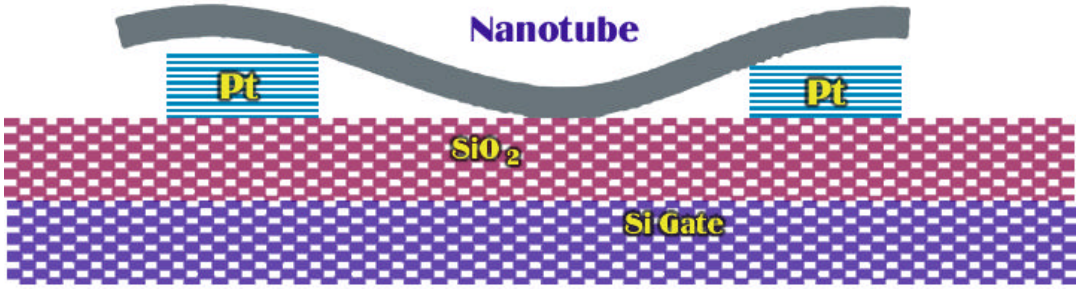
CNT Applications: Electronics



- CNT quantum wire interconnects
- Diodes and transistors for computing
- Capacitors
- Data Storage
- Field emitters for instrumentation
- Flat panel displays
- THz oscillators



Challenges

- Control of diameter, chirality
- Doping, contacts
- Novel architectures (not CMOS based!)
- Development of inexpensive manufacturing processes

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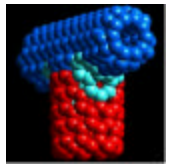
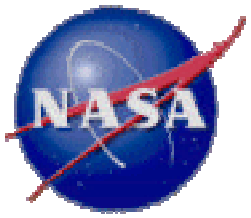
Potential CNT Applications and Challenges



Source: Workshop Report - SRC/NASA Ames Workshop on Emerging Opportunities and Issues in Nanotubes and Nanoelectronics

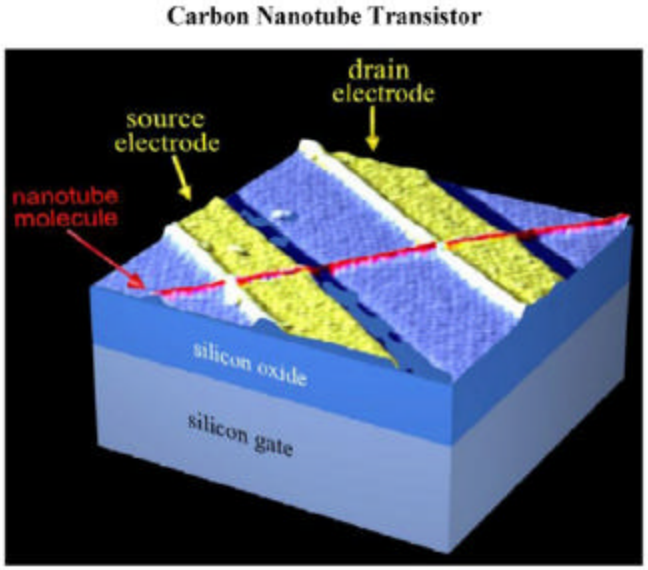
Application	Property	Challenge
CNT for active electronic devices	Possibilities to control electronic properties by structural characteristics	The current standards should be met: low cost (1 µcent/transistor), high level of integration (10^9 transistors /circuit); high reproducibility (+/- 5%), reliability(operating time >10years)
CNT as interconnects	Low resistivity	Manipulation/attachment of individual CNT
Passive devices: capacitors and inductors	Geometrical characteristics	Is it possible to grow helical conducting nanotubes?
Field emitters	High aspect ratio, thermal conductivity	Performance of CNT field emitters ?
CNT-film as a low-K insulator	inherent low density of the CNT-films	The CNT film would need to be deposited, planarized, patterned and etched with techniques compatible with the underlying silicon devices
Probes for metrology	High aspect ratio of tips	Attachment of a single CNT to the cantilever
Manufacturing with Micro- or Nano-Tools	High aspect ratio of tips	Micro-tool arrays must be “fast, flexible, and inexpensive”



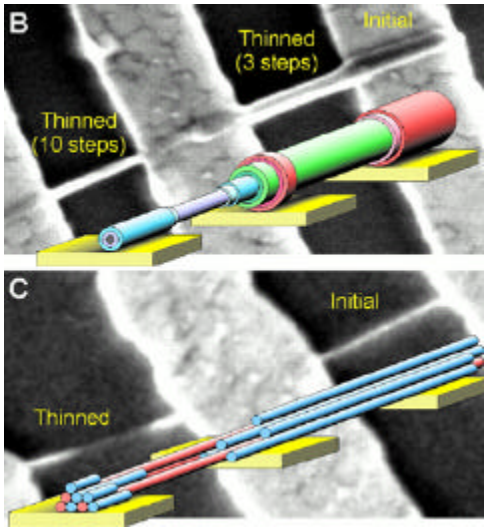
What has been Demonstrated to Date?

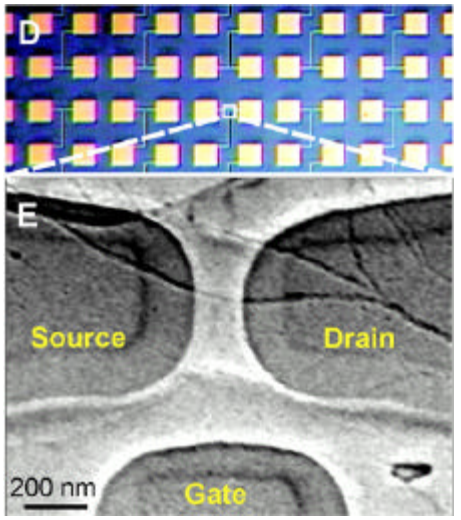
- Doping SWNT with K or Br decreases resistivity by a factor of 30. (Lee et al, -Smalley Group- Nature, July 97)
- 2-probe and 4-probe transport measurements at 300 K showed that nanotubes can behave as a chain of quantum wires connected in series. (Bezryadin et al - Dekker group - DRL, 1998)
- High stable current densities ($> 10^7$ A/cm^2) obtained with MWNTs. Postulated that nanotubes conduct current ballistically and do not dissipate heat. MWNTs were ~ 15 nm diameter and 4 µm long. (Frank et al - de Heer group - Science, 1998)
- Pure MWNT resistivity 5.3 x 10^{-6} - 1.9 x 10^{-5} ? m and B-doped nanotube shows reduced resistivity (7.4 x 10^{-7} - 7.7 x 10^{-6} ? m. In both cases, a decrease in resistivity with increasing temperature was observed $\Rightarrow$ semiconductor - like behavior (Wei et al, APL 1999)
- Room temperature CNT transistor operation: 3 terminal switching device based on one CNT connected to two metal electrodes and controlled by a gate. (Dekker's group & Avouris' group, 1998)

Nanotube Electronic Devices: FETs



Dekker & coworkers, *Nature* **393**, 49 (1998)



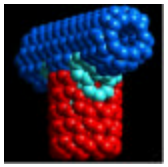


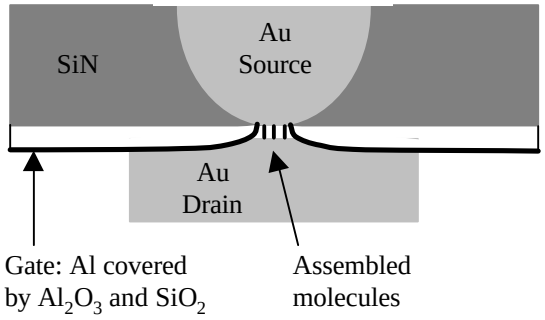
Avouris & coworkers, *Science* **292**, 706 (2001)

- Semiconducting nanotubes can function as field effect transistors with large on/off ratios and relatively high mobilities.
- Uncontrolled synthesis of metallic and semiconductor nanotubes places significant contraints on assembly of device arrays.

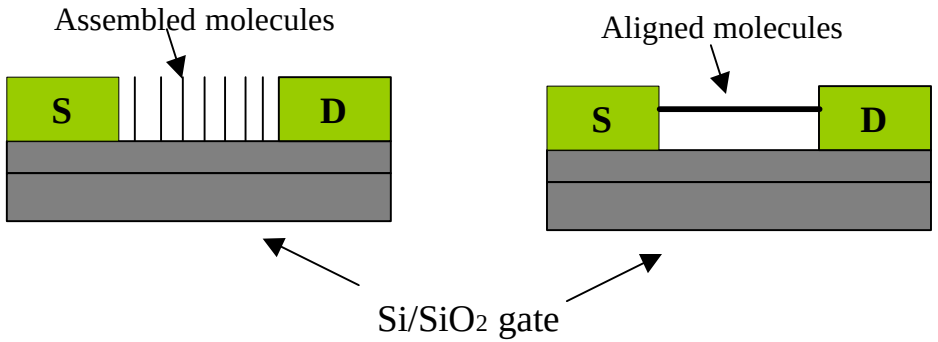
Courtesy - Lieber

Device Design and Fabrication





Nanopore structure



Field effect transistor structure

mature fabrication technology

- nanolithography (Stanford, Cornell and UCSB)
- self assembly (in house)

technology under development

- molecular alignment between two electrodes
- interconnects

Carbon Nanotube Transistor Fabrication

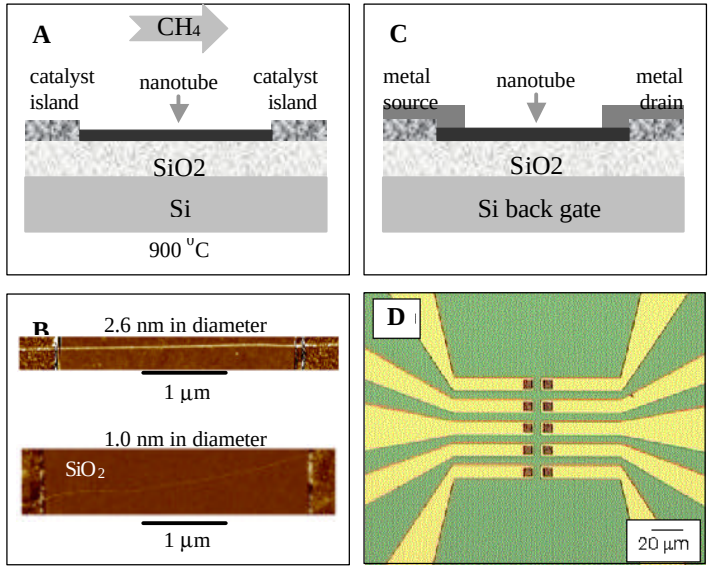


Figure 1 Inllustration of our synthetic and fabrication approach. (A) A single-walled carbon nanotube is grown bridging two adjacent catalyst islands via chemical vapor

A. A single wall carbon nanotube is grown bridging two adjacent catalyst islands via chemical vapor deposition of methane at 900C
B. Atomic force microscope (AFM) images of two as-grown nanotubes on silicon oxide surface
C. Metal is deposited to cover both ends of the nanotubes and serves as the source and drain electrodes
D. Optical image of five potential nanotube devices showing the catalyst islands (dark squares)

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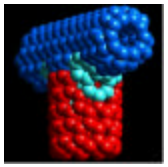
From p- to n-type nanotube MOSFET transistor



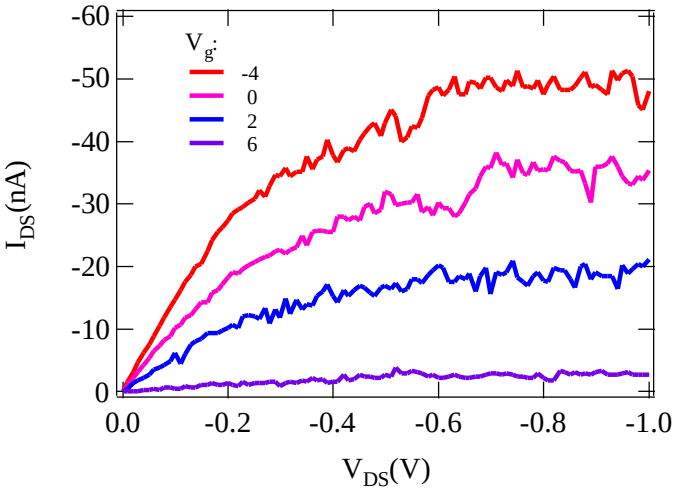
Both n- and p-transistors are needed for logic devices

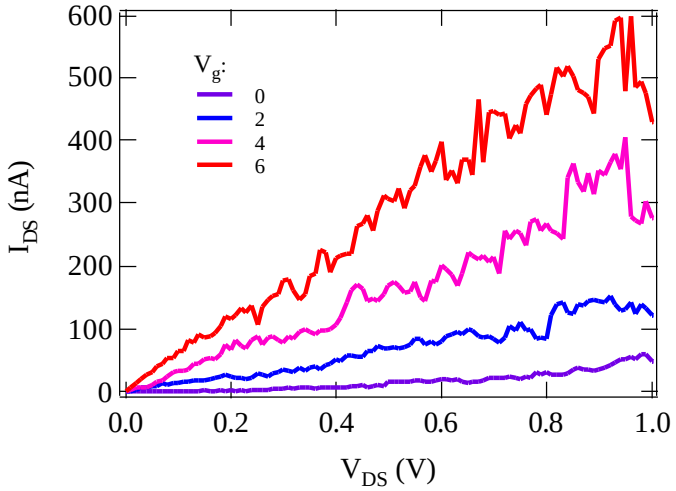
Previous work: p-nanotubes

1. **Oxygen adsorbed**
2. **Si/SiO_2 gate**

Present work: n-nanotubes

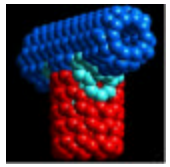
1. **Potassium adsorbed or**
2. **Si/TiO_2 gate**



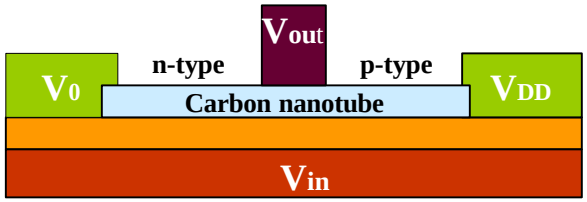


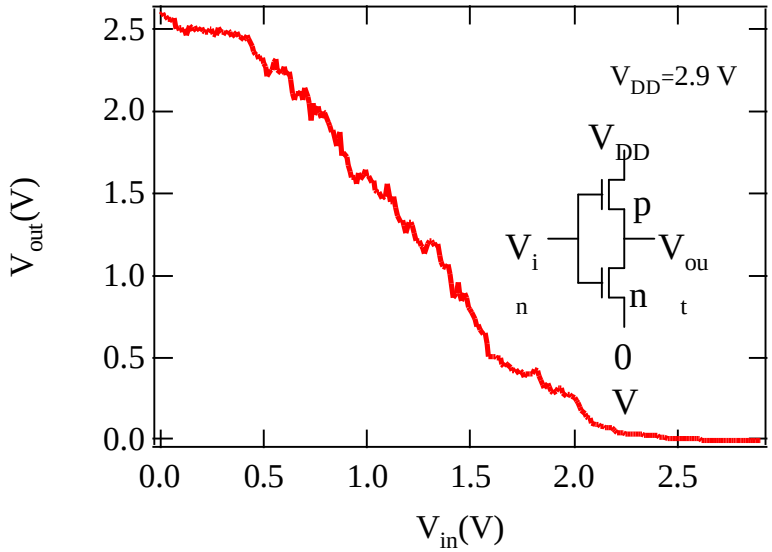
(manuscript in preparation)

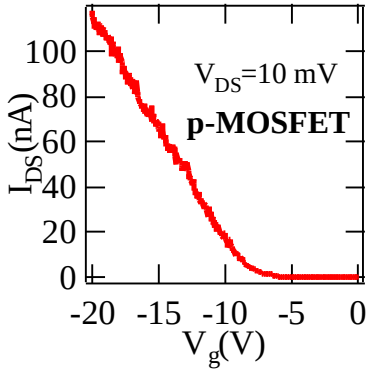
Logic and Memory Devices

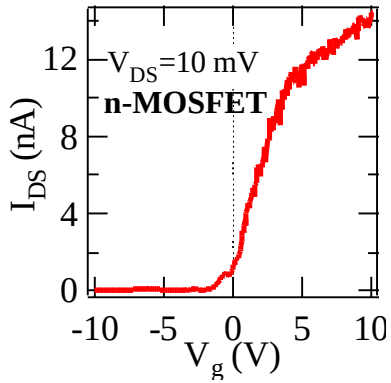


First single nanotube logic device – Inverter demonstration

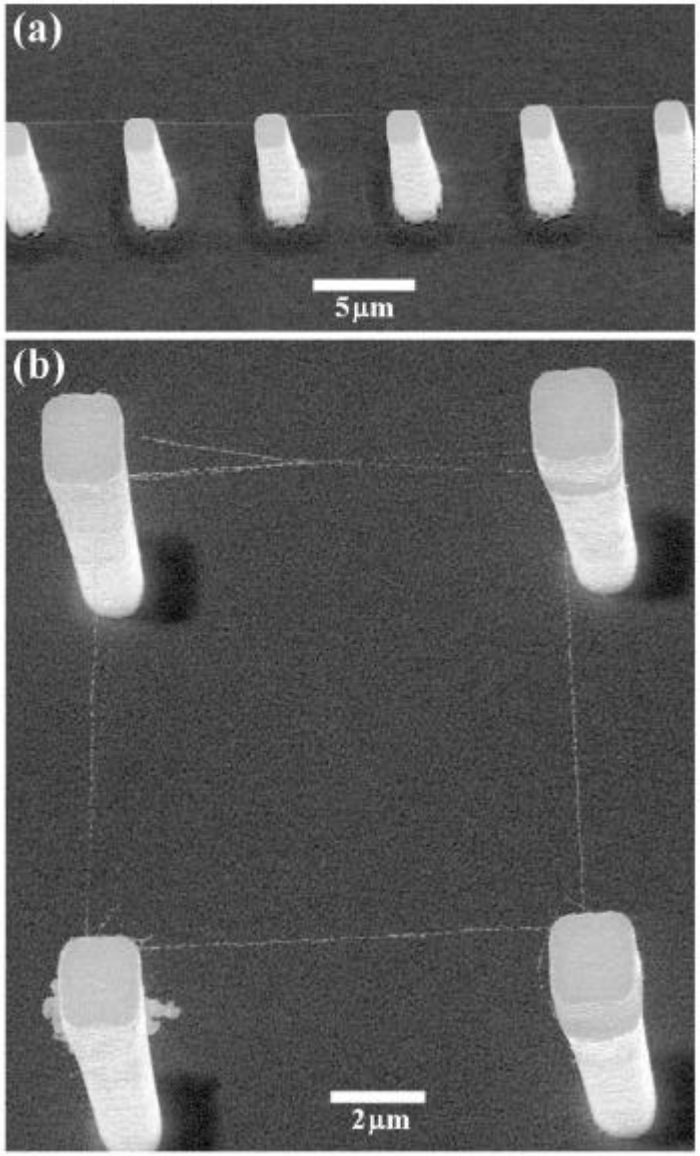








Nanotube Device Fabrication by CVD

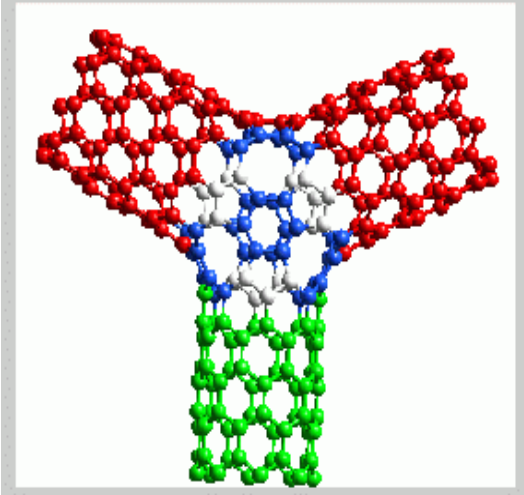


CVD allows patterned growth and organization of nanotubes for device fabrication.

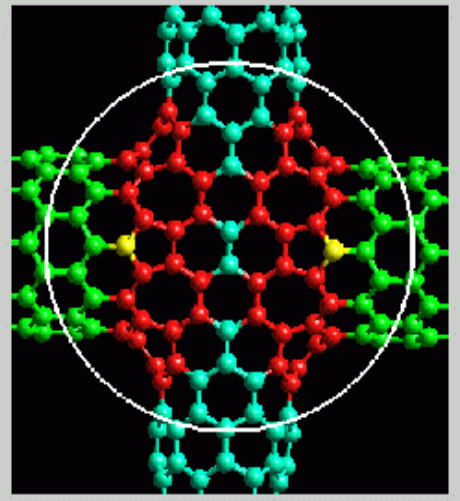
Scale-up for large scale assembly of transistors using this may not work.

Multi-terminal Nanotube Junctions

Pathways to Two Dimensional Molecular "Networks"



Metal–Semiconductor–Metal
"Y" Tunnel Junction



A four–terminal nanotube heterojunction

"It turns out that all of our proposed junctions satisfy – Generalized Euler's Rule about the global topology of connected networks"

M. Menon and D. Srivastava, J. Mat. Res. Vol. 13, 2357 (1998)
D. Srivastava, S. Saini and M. Menon, *Molecular Electronics,* Ed. Aviram and Ratner, 178 (1998)

Multi-wall Y-junction Carbon Nanotubes

Experimental Synthesis of Multi-wall Carbon Nanotube Y-Junctions (2000)

VOLUME 85, NUMBER 16 PHYSICAL REVIEW LETTERS 16 OCTOBER 2000

Electronic Transport in Y-Junction Carbon Nanotubes

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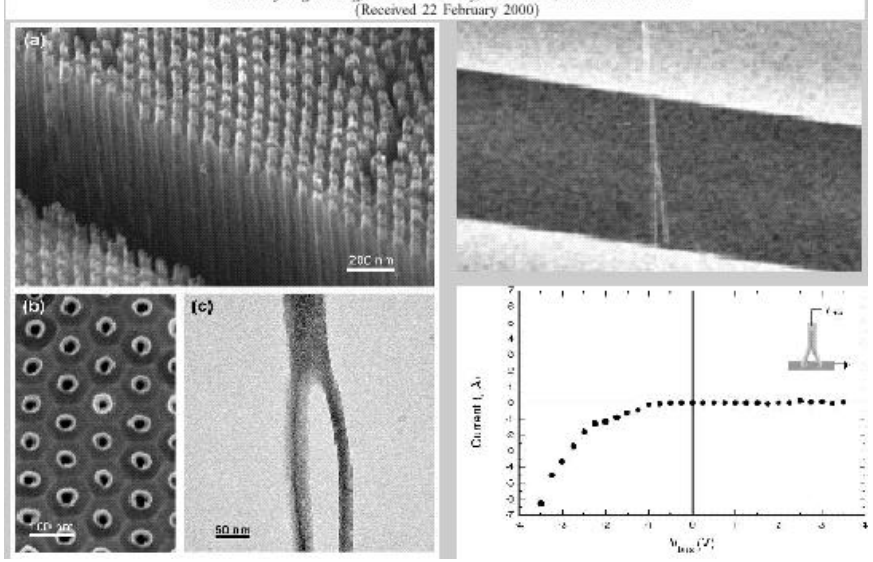
(Received 22 February 2000)



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Y-junction carbon nanotubes

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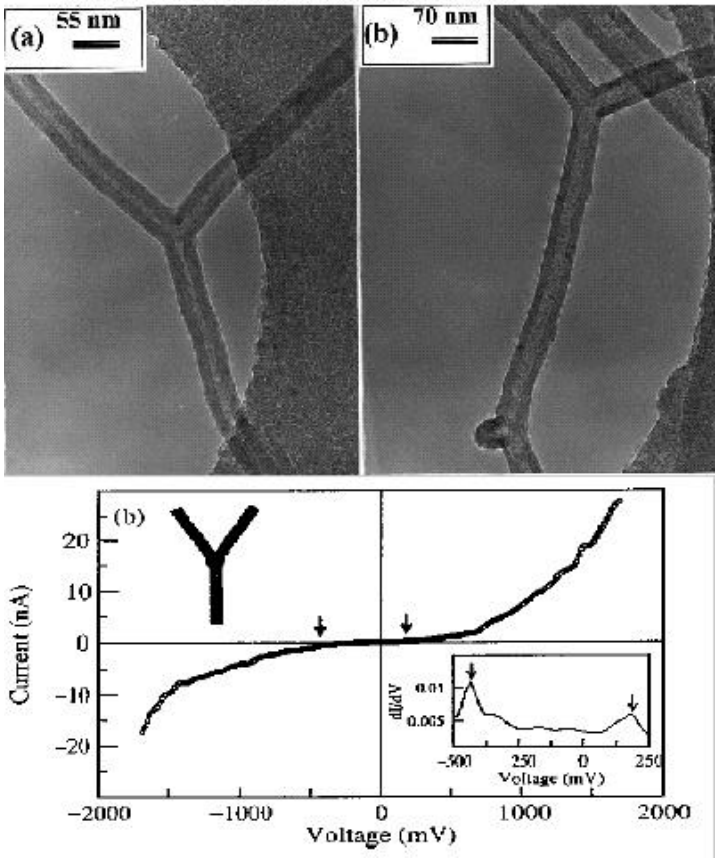
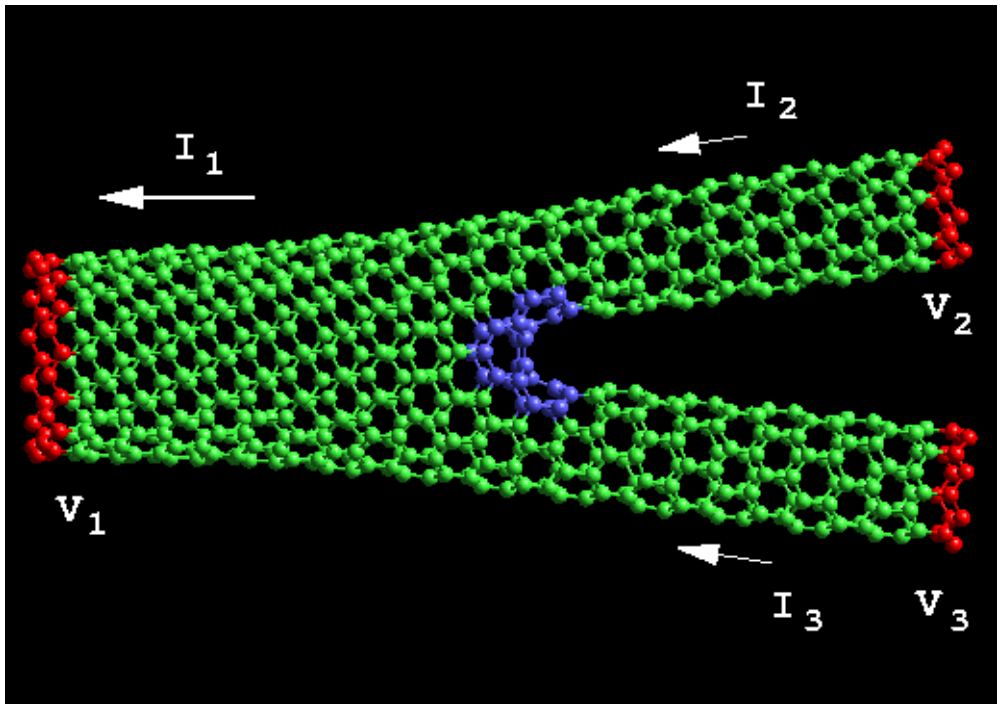
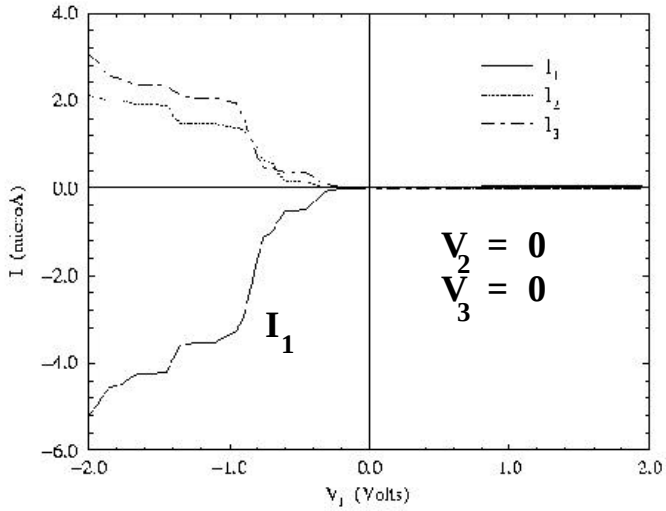
(Received 11 July 2000; accepted for publication 28 August 2000)

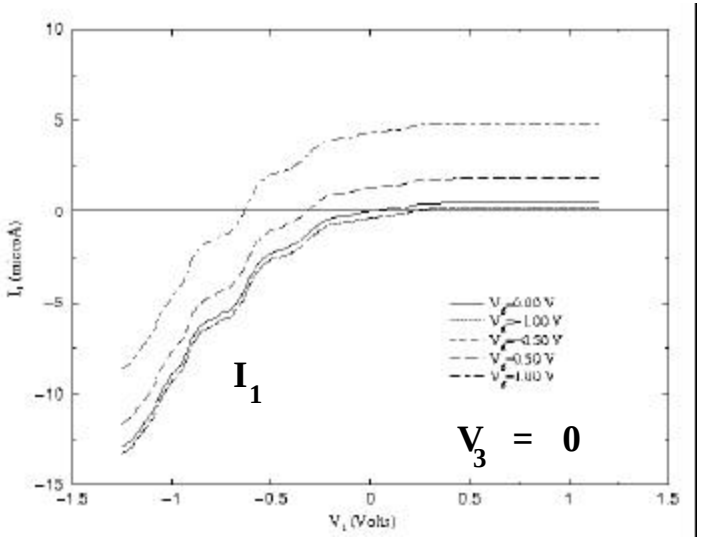


Transport in Y-junction Carbon Nanotubes

Rectification and Ballistic Quantum Transport in Carbon Nanotube Y junction

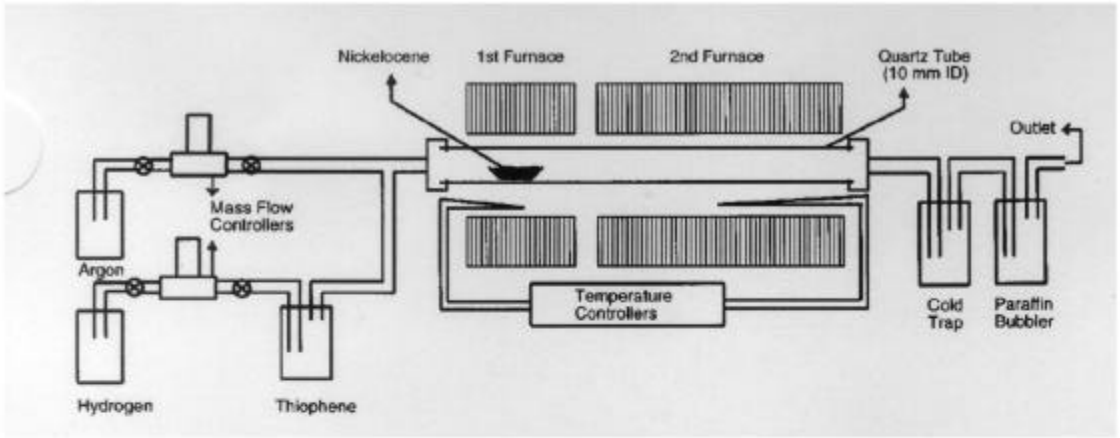


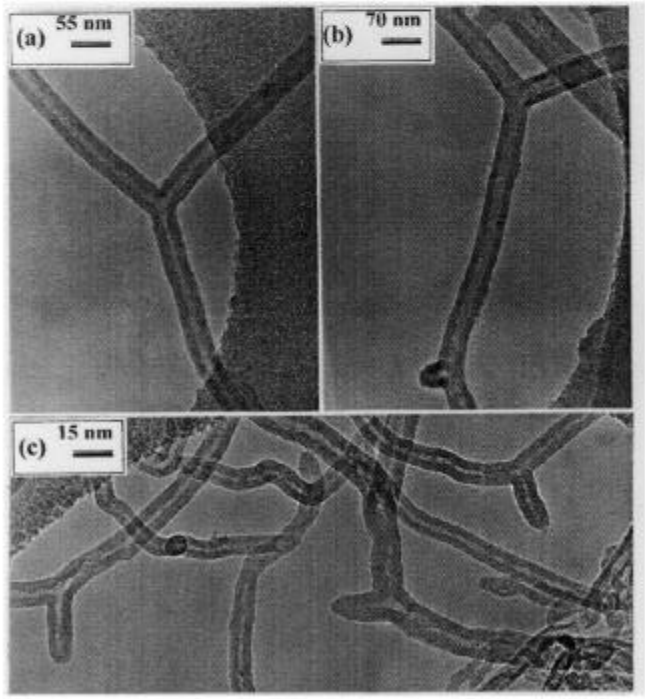


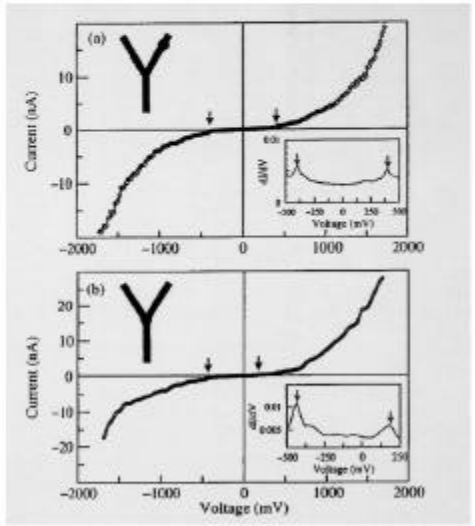


A Andriotis, M. Menon, D. Srivastava and, L. Chernozatonski, submitted, Phys. Rev. Lett. (2001)

CVD Production of Y-Juntions







C.N.R. Rao and co-workers,
APL, Vol. 77, 2530 (2000).

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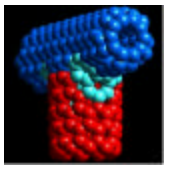
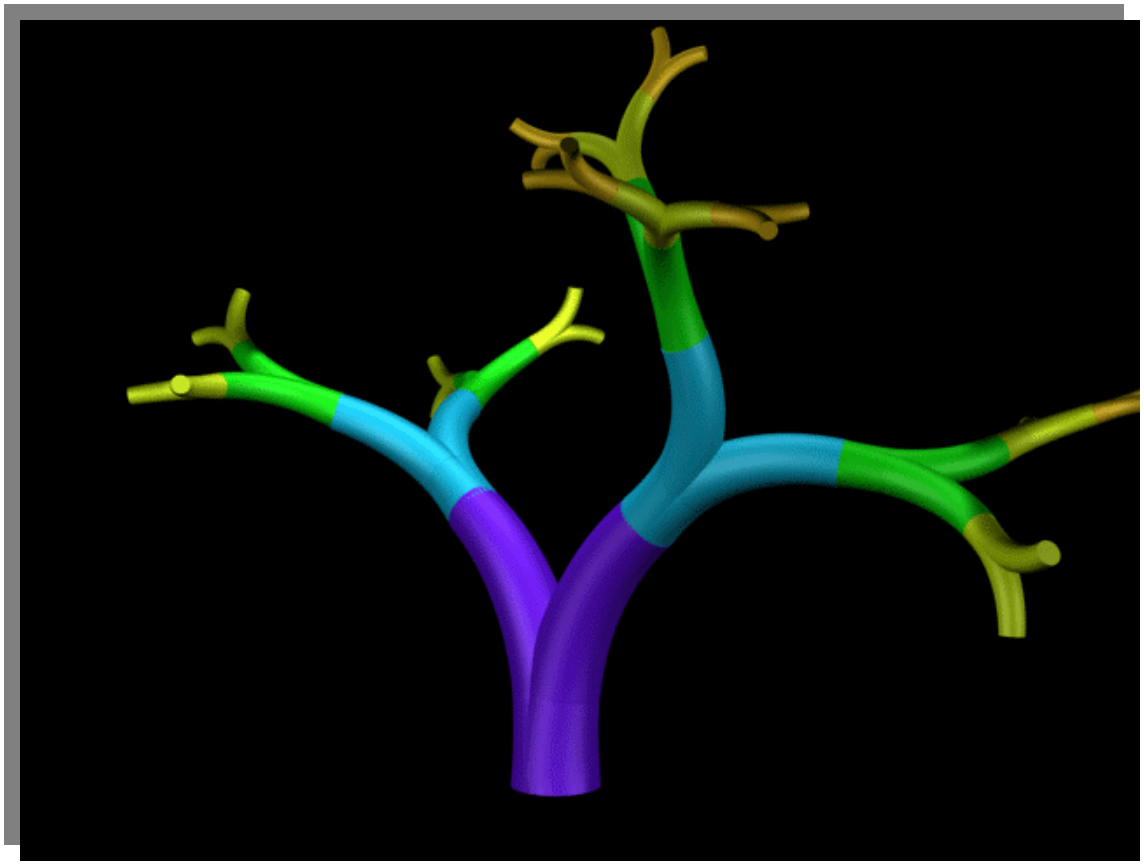
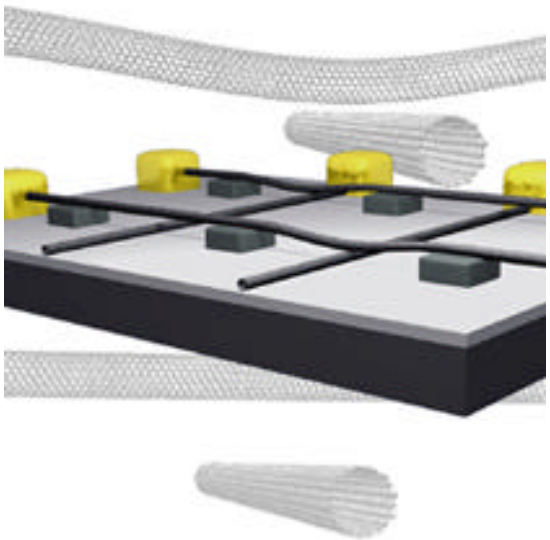
Four-level CNT Dentritic Neural Tree

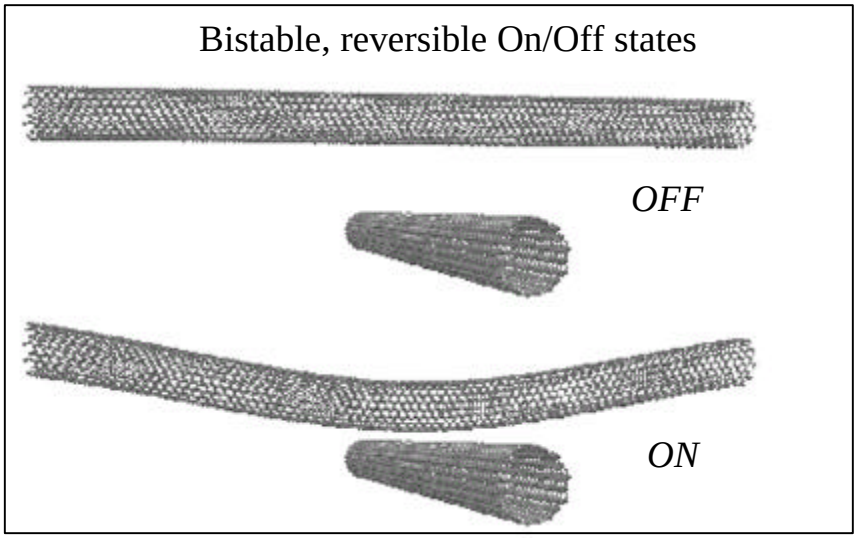


- Neural tree with 14 symmetric Y-junctions
- Branching and switching of signals at each junction similar to what happens in biological neural network
- Neural tree can be trained to perform complex switching and computing functions
- Not restricted to only electronic signals; possible to use acoustic, chemical or thermal signals



Nanotube Electromechanical Devices



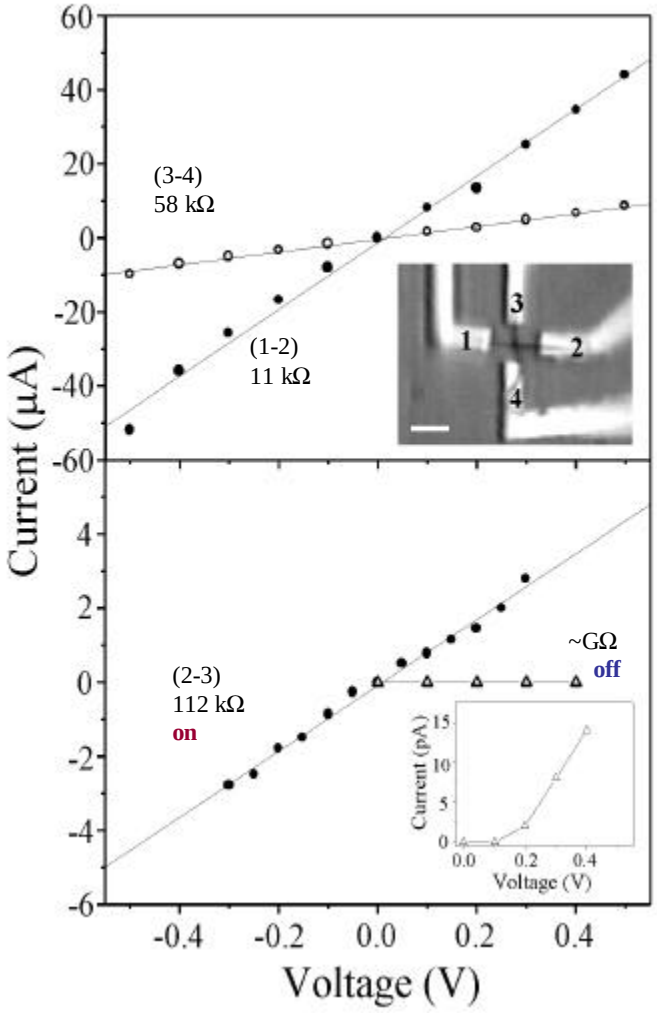


Lieber and coworkers, *Science* **289**, 94 (2000)

- **Nonvolatile** RAM: bistable and switchable at room temperature
- **Robust** read-out: large on/off conductance change
- **Parallel** addressability of memory elements
- **Reliable**: efficient heat dissipation; no electrical/mechanical failure
- **Speed**: ~ 200 GHz (τ_{mech}, τ_{RC})
- **Integration level**: ~ 10^{12} bits/cm^2

Courtesy - Lieber

Nanotube Device: Proof of Concept

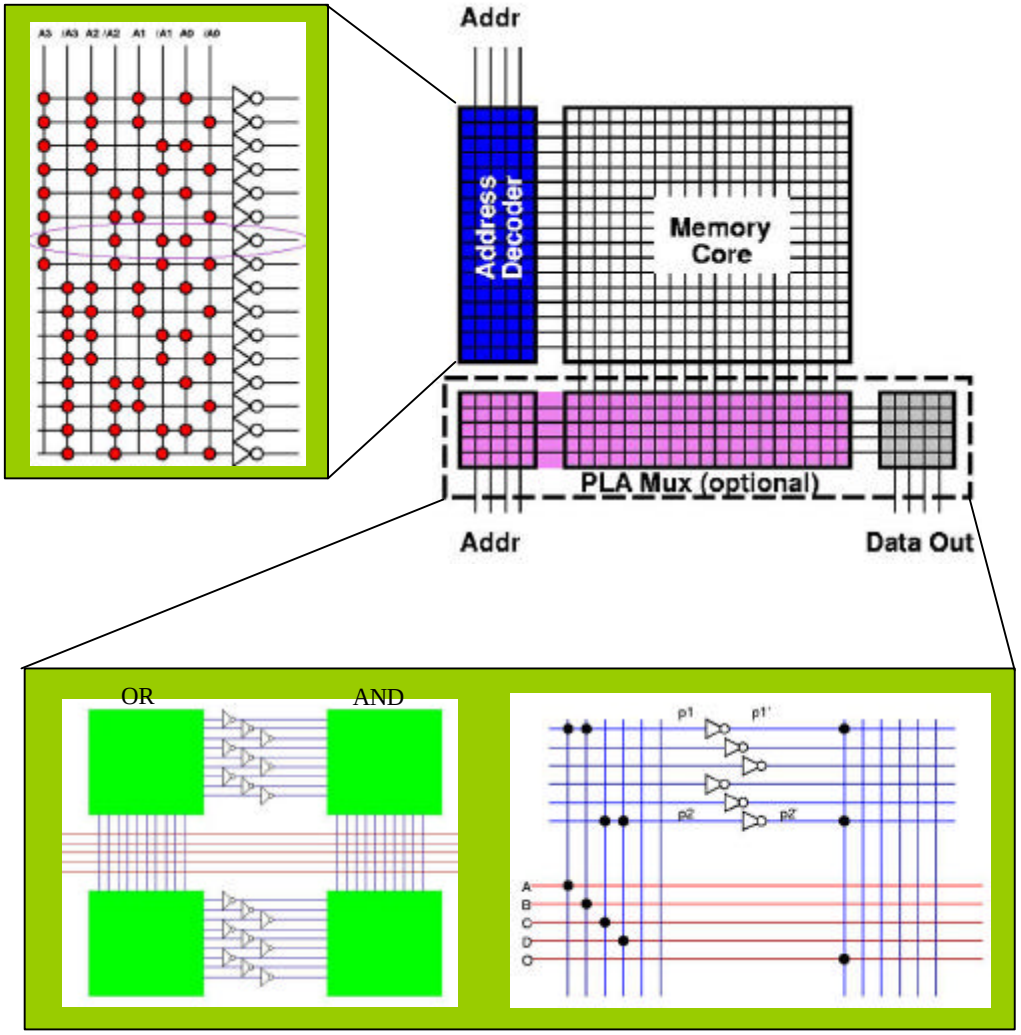


- SWNT bundles are assembled onto electrodes that define a suspended structure.
- Individual SWNTs in ohmic contact with electrodes
- Junction resistance: $R_{OFF}/R_{ON} \sim 10^5$
- ON: ohmic
- OFF: tunneling

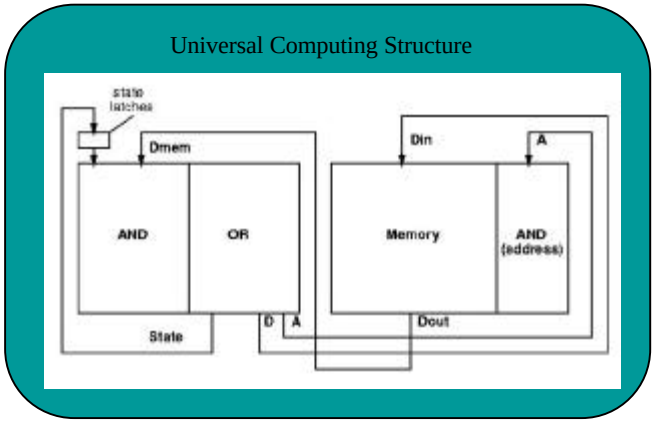
Rueckes, Kim, Joselevich, Tseng, Cheung & Lieber, *Science* **289**, 94 (2000)

Courtesy - Lieber

Towards Memory and Computation



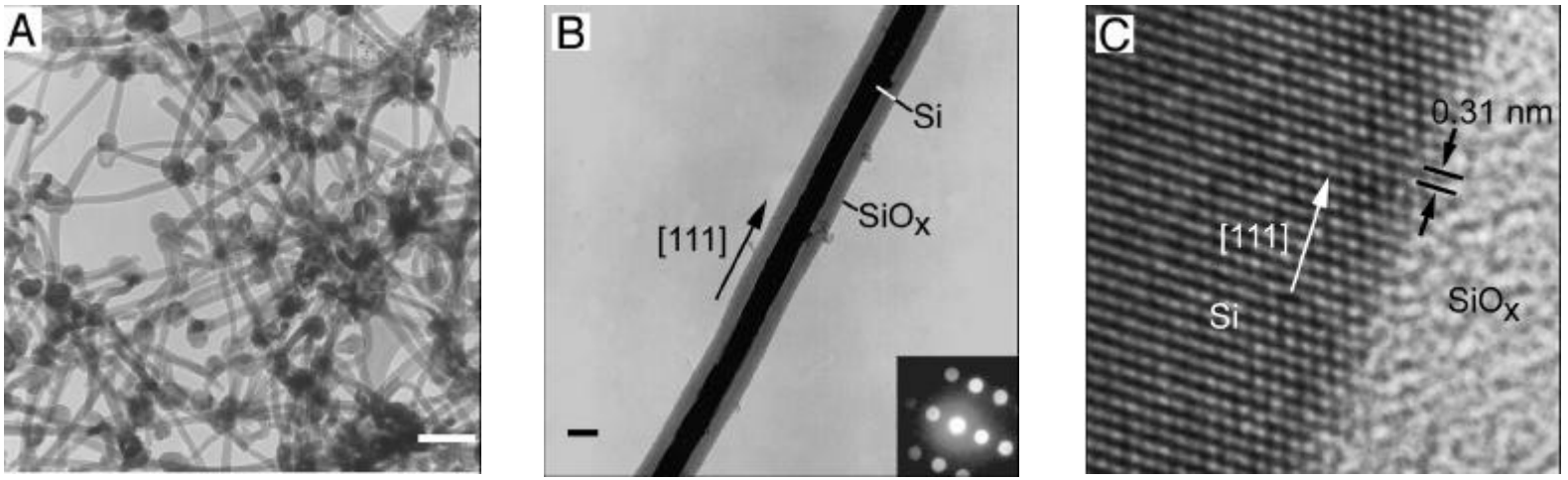
- Nonvolatile memory core can be readily obtained from a suspended nanotube array.
- Reading and writing can be carried out using programmable logic arrays (PLAs) based on the nanotube architecture.
- Memory and PLA structures could be combined to implement universal computing machines.



DeHon & Lieber, 2000

Courtesy - Lieber

Growth of Silicon Nanowires



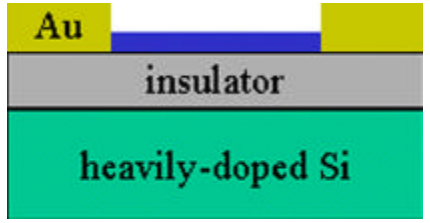
Morales & Lieber, *Science* **279**, 208 (1998)

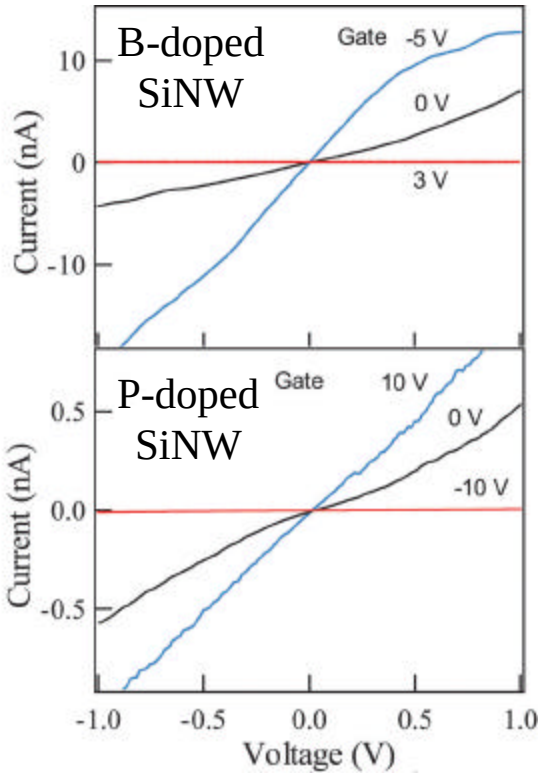
- Laser ablation of $Si_{0.9}Fe_{0.1}$ at 1200 ^{o}C leads to a high yield of material with wire-like morphology.
- TEM analysis demonstrates that nanometer diameter wires consist of a crystalline silicon core encased in an amorphous silicon oxides sheath.

Courtesy - Lieber

Nanowire Building Blocks

- Electrical properties defined using three-terminal measurements.
- Carrier concentration in p- and n-type materials can be varied by several orders of magnitude.
- Nanowires can be turned on and off with gate voltage–they are field-effect transistors.

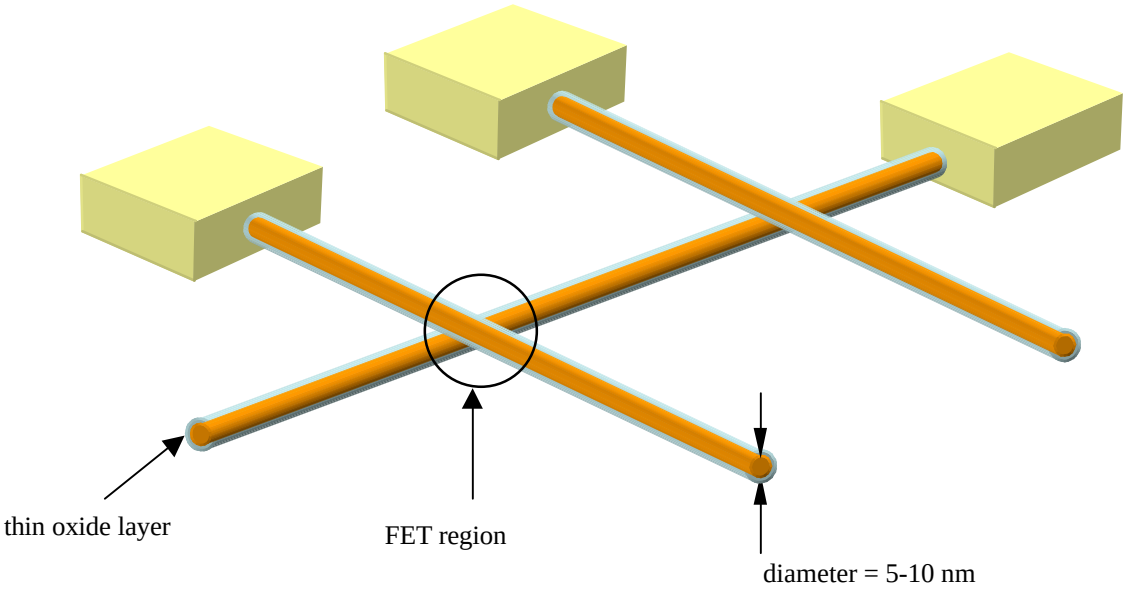




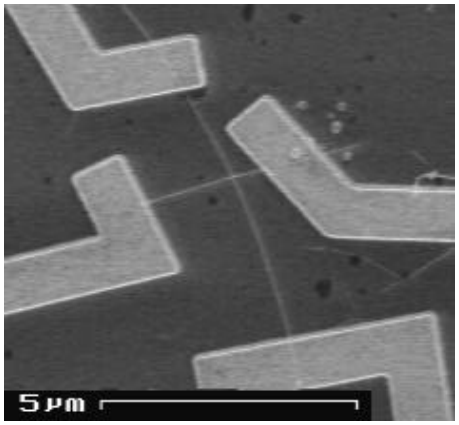
Lieber & coworkers, *J. Phys. Chem. B*, **104**, 5213 (2000)
Lieber & coworkers, *Nature* **409**, 66 (2001)
Cui & Lieber, *Science* **291**, 851 (2001)

Courtesy - Lieber

Nanowire Transistors with Nanogates



SEM image of a prototype device

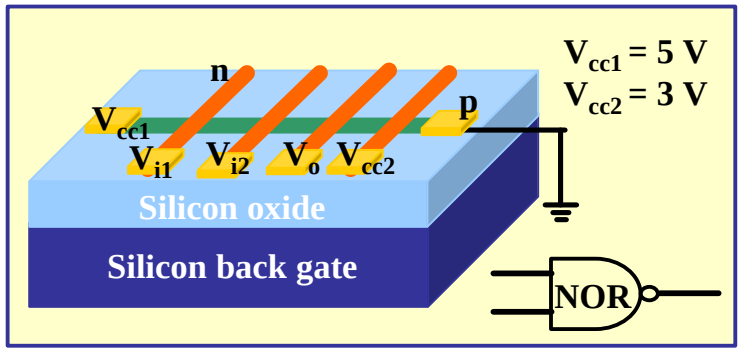


- Nanoscale transistors can solve routing problems in 2D array structures.
- Back(global) gating switches every element in the device (no selectivity)
- Controlled oxide layer surrounding nanowires functions as gate oxide.
- Small gating area enables fast switching and low switching voltage

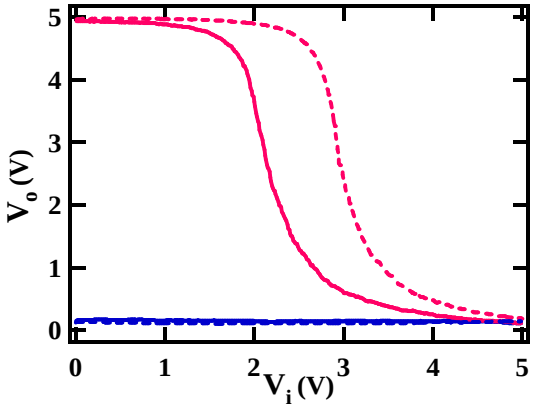
Kim & Lieber (2001)

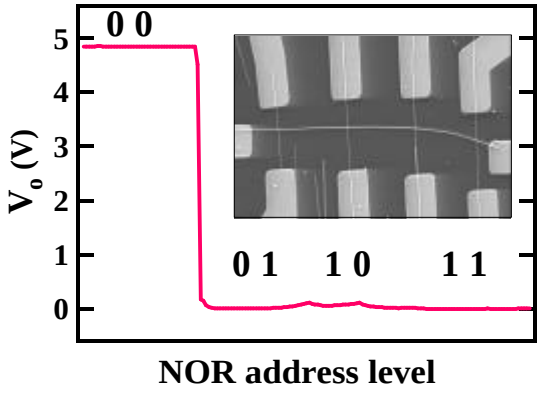
Courtesy - Lieber

Logic Gate “NOR”



V_{i1}	V_{i2}	V_o
0	0	1
0	1	0
1	0	0
1	1	0

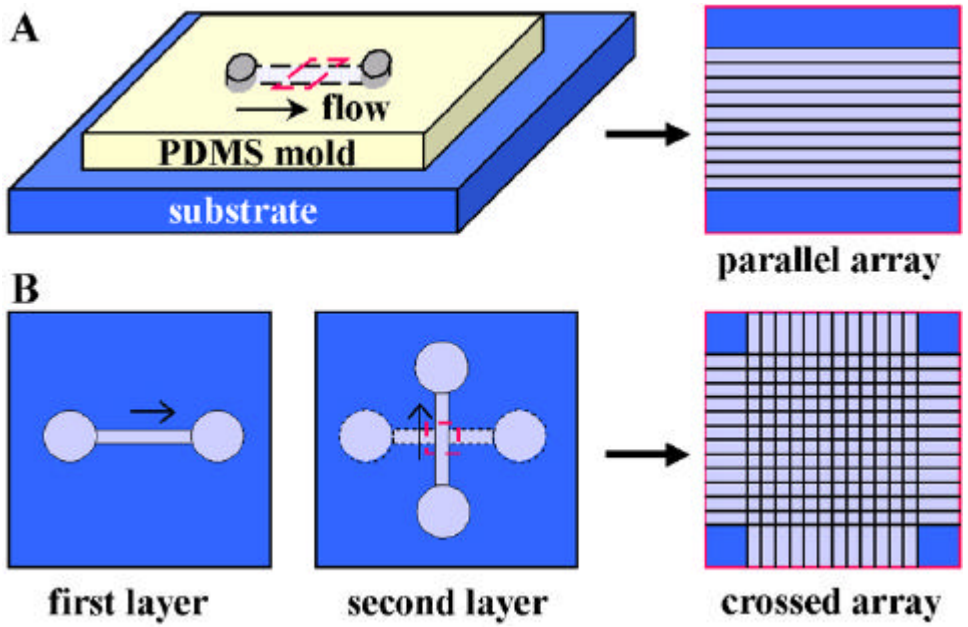




Courtesy - Lieber

Hierarchical Assembly of One Dimensional Nanostructures

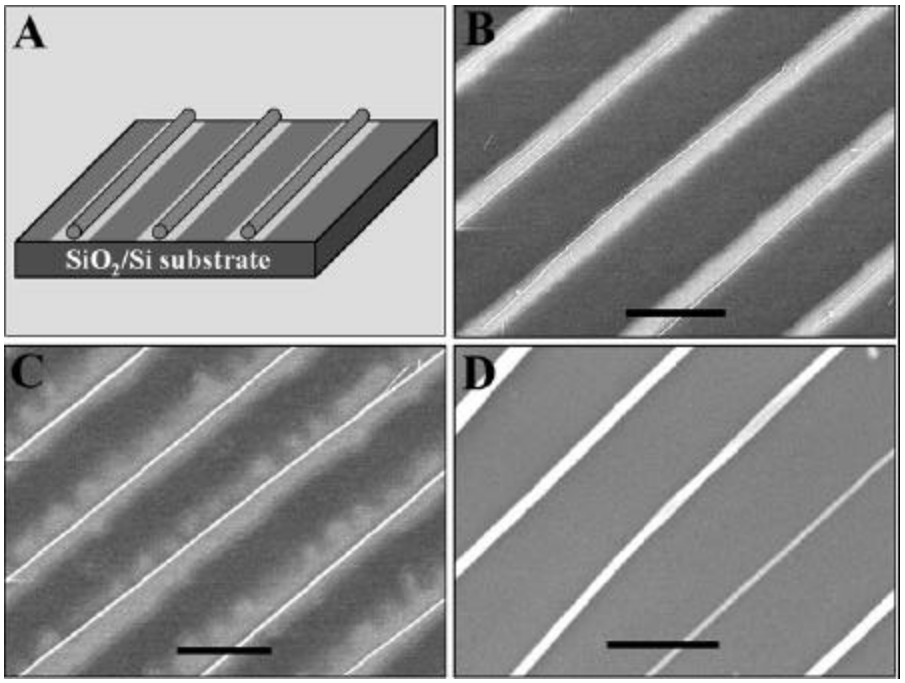
- Moving beyond studies of single devices to future nanosystems will require development of efficient and scalable strategies for hierarchical assembly.
- Fluidics represents one approach that can organize nanowires and nanotubes into functional networks.

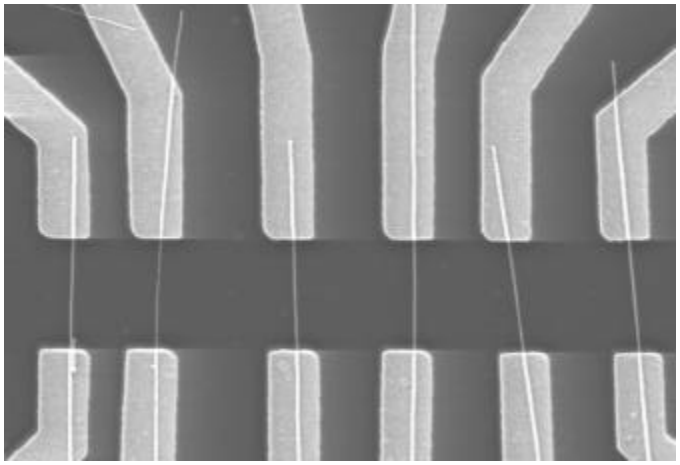


Huang, Duan, Wei & Lieber, *Science* **291**, 630 (2001)

Courtesy - Lieber

Directed Assembly of Parallel Arrays



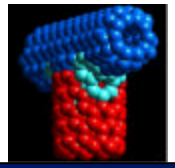


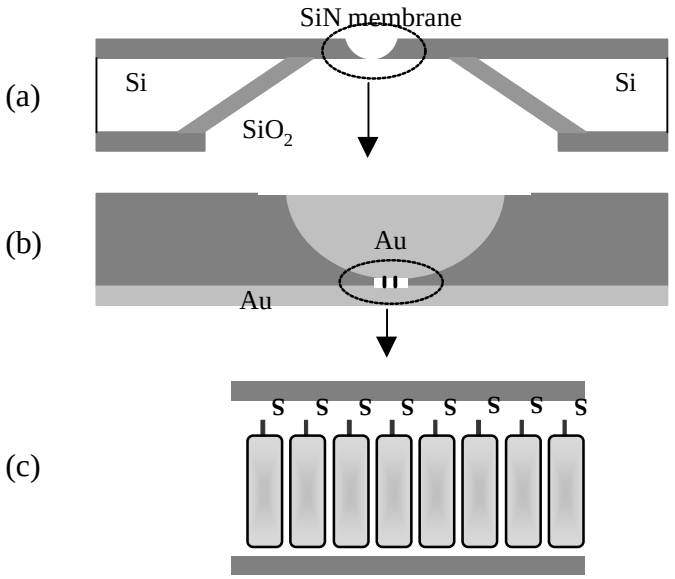
- Fluidic assembly on patterned surfaces enables control of the alignment and periodicity of assembled nanowires over many length scales.
- Electrically-addressable parallel arrays can created by subsequent metal depostion, or by assembly on predefined electrode arrays.

Courtesy - Lieber

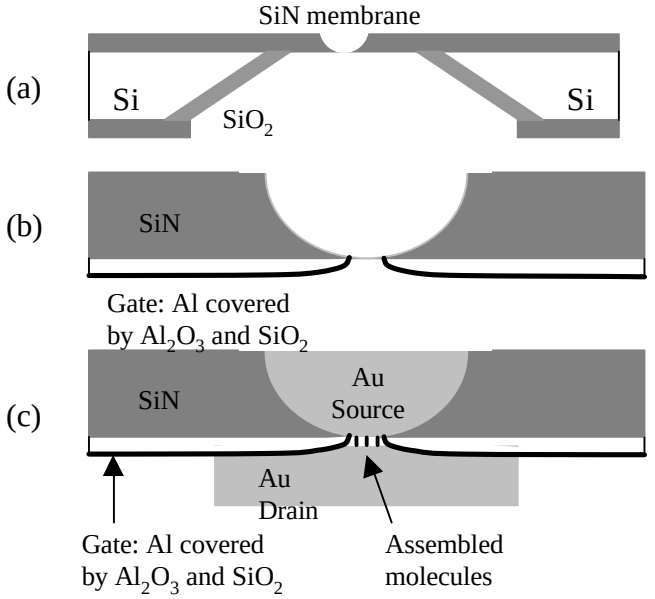
Ames Research Center

From two to three terminal moletronics devices



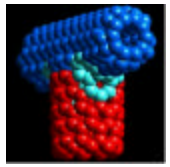


(a) Cross section of a silicon wafer showing the bowl-shaped pore etched in the suspended SiN membrane with a diameter 20 ~ 30 nm. (b) Au / self-assembled monolayer / Au sandwich structure in the nanopre. (c) Detail diagram of the sandwich structure. Shaded boxes represent the molecular components of the organothiol thin film.

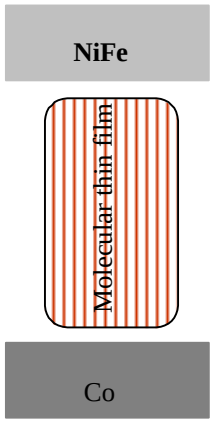


(a) The starting substrate with suspended silicon nitride membranes. (b) Aluminum is deposited from the flat side of the membrane, followed by oxidation of the surface and deposition of a layer of SiO_2 to provide electrical isolation. (c) Gold is deposited from the top side to fill up the pore, followed by deposition of molecular wires and finally deposition of gold from the bottom to work as the drain electrode.

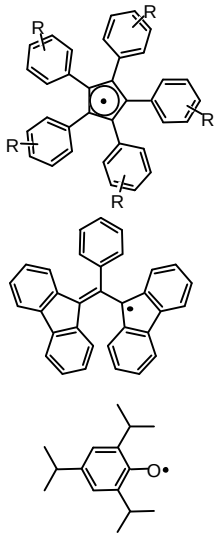
From Moletronics to Spintronics devices



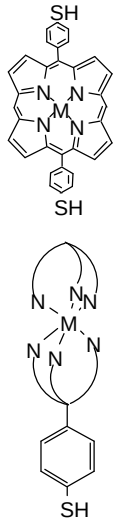
(a) Spintronic devices



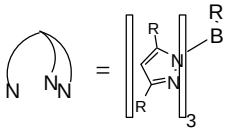
(b) Radial materials

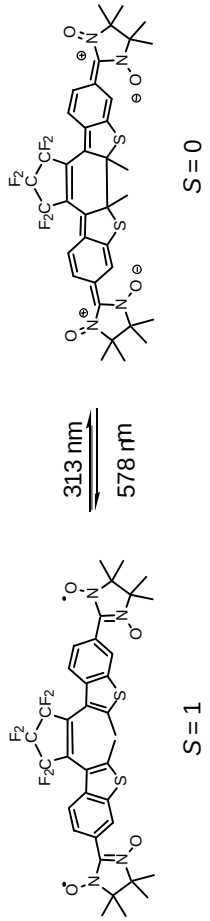


(c) Inorganic complexs



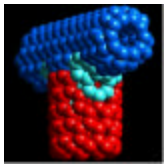
(d) Photoswitchable diradical



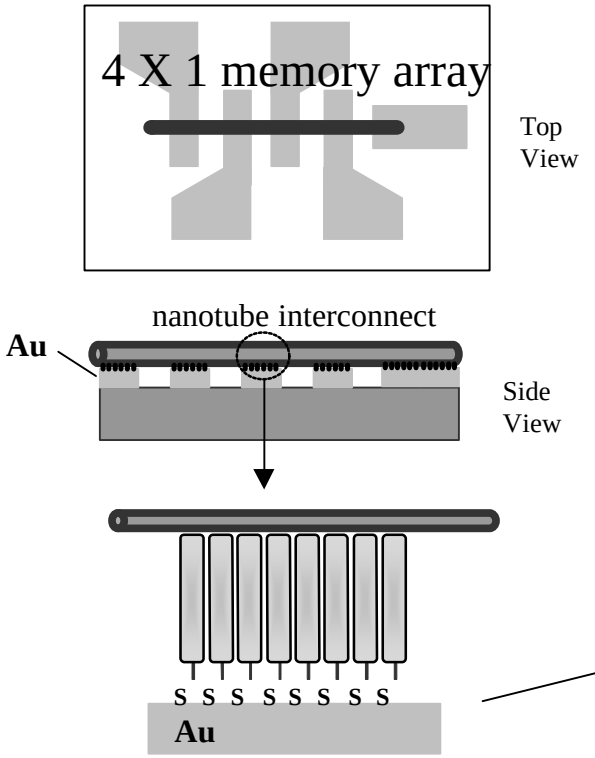


Moletronics fabrication technology will be used to make molecular spintronics for exploration of enhanced memory and quantum computing devices.

Logic and Memory Devices

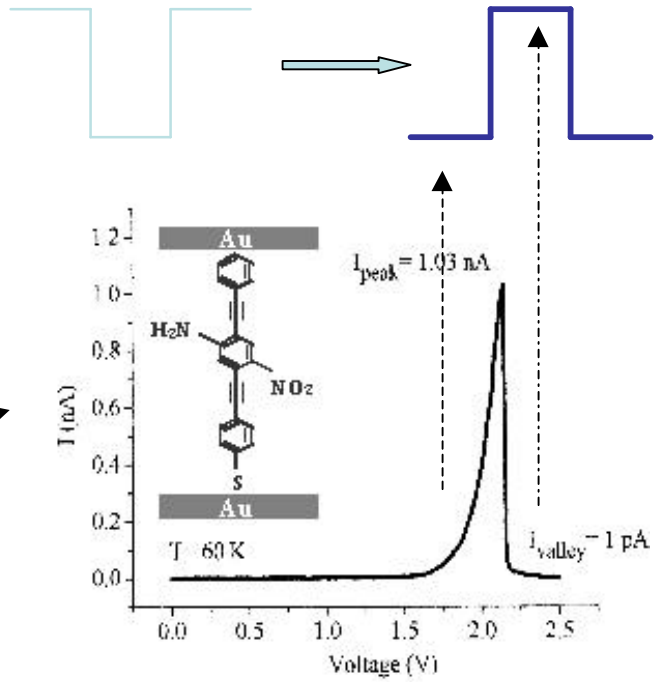


Molecular Memory – demonstration work in progress



Write:
Apply + / -
Voltage

Read:
Measure junction resistance



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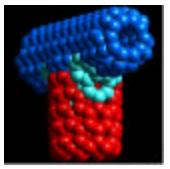
Semiconducting Nanowires



- Semiconducting materials such as Si, GaAs, InP, GaN… can be grown into nanowires (~ 10 nm diameter, microns long)
- Catalyst mediated growth unlike in thin film or bulk crystal growth
- Carbon nanotube growth has yet to achieve selectivity between semiconducting and metallic tubes which is not the issue with NWs
- NWs useful for devices and sensors
- Lieber (Harvard) has made significant progress

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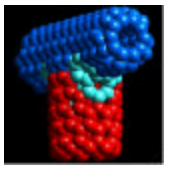
Hardware and Architectures



- In nanoelectronics - whether based on nanotubes, nanowires, organic molecules or DNA - useful designs of architectures and hardware are not clear/known yet.

- Designing the only-known CMOS architectures with molecular electronics devices 100-1000 times smaller than today's CMOS may not be of value.

- "Eventually, we will need to know how to design hardware when we have no idea how to do it."

  - David Fogel, Editor, IEEE Trans. Evolutionary Computation, 1977 in describing evolvable hardware

Molecular electronics meets needs evolvable hardware

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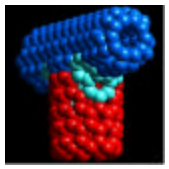
Concluding Remarks



- Nanotechnology has a few alternatives for silicon based electronics if and when the silicon engine runs out of steam: C nanotubes, NWs, organic or DNA based moletronics
- Basic device demonstrations and simple logic functions are encouraging and keep optimism alive 
- Low cost self-assembly or bottom-up manufacturing is the real target; failure here will doom nanotechnology in nanoelectronics 
- System architecture design is key which will demand revolutionary approaches